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SEMICONDUCTOR TEST APPARATUS AND

CONTROL METHOD THEREFOR

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor test apparatus that optimally
distributes pattern files necessary for the testing of the operation of the semiconductor to
be tested (a semiconductor integrated circuit) in executive memory.

Description of the Related Art

In semiconductor test apparatuses, the pattern data necessary for carrying out
the test of the semiconductor comprises the data applied to the semiconductor and the
comparative data that, based on this applied data, evaluates the output data that is output
from the semiconductor.

In addition, when carryout out the testing of the semiconductor, the
semiconductor test apparatus reads the pattern files corresponding to this semiconductor
from a high-capacity memory apparatus, and stores these in the memory of the test
apparatus as pattern files.

Here, referring to Fig. 4, the manner in which the conventional semiconductor
test apparatus controls these pattern files will be explained.

Before the start of the test, the control unit 40 stores the pattern files from an external
memory apparatus (not illustrated) that are used in the testing of a plurality of types of
semiconductors in the DISK 42 built into the semiconductor test apparatus 41.

Next, in the preparation stage of the test of the semiconductor, the control unit 40 transfers the pattern files for testing the type (type 1) of semiconductor that will be tested to the high-capacity buffer memory 43 of the semiconductor test apparatus 41 from the DISK apparatus 42 as pattern files having the same format as when stored in the DISK apparatus 42, and stores them.

Normally, during the test of the semiconductor, a plurality of pattern files corresponding to the test items for each type of semiconductor is prepared, and as a result, a plurality of pattern files is stored in the DISK 42 and the buffer memory 43.

In the state wherein the pattern files are stored in the buffer memory 43 as described above, when the test of the semiconductor begins, the test progresses up to the stage in which a specific pattern file is used among the test items that test a specific operation of the semiconductor.

At this time, the control unit 40 distributes pattern data used in the test and control data that controls the operation during the test from the pattern files that relate to specific test items.

In addition, the control unit 40 transfers this distributed data to the pattern memory 44, the MIC memory 45, and the SPG (Serial Pattern Generator) memory 46, which comprise the executive memory while the test of the semiconductor is being carried out.

Here, the pattern memory is memory for storing the pattern data for the test of the semiconductor, the MIC memory 45 is the memory for storing the control data that controls the operation of the semiconductor test apparatus, and the SPG memory is memory that stores the pattern data, which sends the pattern of a periodic clock to a terminal of a semiconductor.

This means that the data for the pattern files is distributed in each executive

memory (comprising the pattern memory 44, the MIC memory 45, and the SPG memory 46), and the control unit 40 controls these files as linked data sets based on a specific algorithm.

Next, the file control algorithm in the above-mentioned executive memory (pattern memory 44, MIC memory 45, and SPG memory 46) according to the conventional technology will be explained referring to Fig. 5.

Fig. 5 is a flowchart that shows the operations of searching the pattern files, transferring the pattern files to the executive memory, and finally implementing the test based on pattern files for one among the test items for testing the semiconductor.

In step 51, for the semiconductor to be tested, the control unit 40 searches the pattern files to be used in testing the semiconductor in each executive memory, and in step 52 the control unit decides whether or not this pattern file is present in each executive memory.

As a result of this decision, in the case that the pattern file is already present in the executive memory, the processing jumps to step 5D, and the test of the semiconductor is started using this pattern file.

Here, in the case that the pattern file used in testing the semiconductor is not present, the control unit 40 distributes it by transferring the necessary pattern files to each executive memory from the buffer memory 43 according to the sequence from step 53 to step 5C.

In step 53, the control unit 40 finds whether or not the relevant pattern files are present in the buffer memory 43, and in the case that the pattern files are not stored in the buffer memory 43, the test of the semiconductor is discontinued by error processing.

In contrast, in the case that the pattern files are present in the buffer memory 43, in the sequence from step 55 to step 5A, the control unit 40 obtains the control